**WHAT IS CLAIMED IS:**

1. A fractional-type phase-locked loop circuit, for synthesizing an output signal multiplying a frequency of a reference signal by a selected fractional conversion factor, the phase-locked loop circuit including:

a frequency divider for generating a feedback signal dividing the frequency of the output signal by a frequency division factor selectable among at least two different integer-value division factors;

frequency divider control means for causing the frequency division factor to vary between the at least two integer-value division factors in a pre-defined number of cycles, wherein an average frequency division factor over said pre-defined number of cycles has a fractional value;

means for compensating a phase error introduced by the frequency divider on the basis of a value indicative of the phase error obtained from said frequency divider control means, wherein said phase-error compensation means includes rounding means said rounding means receiving an input binary code with a first number of binary digits, indicative of the phase error value, and providing an output binary code with a second number of binary digits lower than the first number of digits, the output binary code defining a rounded phase error value.

2. The fractional-type phase-locked loop circuit of claim 1, in which said rounding means includes:

means for separating the input binary code into a first group of binary digits, containing the less significant binary digits of the input binary code, and a second group of binary digits, containing the most significant binary digits of the input binary code; and

means for generating the output binary code by rounding a value defined by the second group of binary digits according to a rounding value defined by the first group of binary digits.

3. The fractional-type phase-locked loop circuit of claim 2, in which the rounding means include an adder for adding a value defined by at least one of the most significant digits of the first group of binary digits to a value defined by the second group of binary digits.

4. The fractional-type phase-locked loop circuit of claim 2, in which the rounding means further include a delta-sigma modulator receiving the first group of binary digits and generating the rounding value.

5. The fractional-type phase-locked loop circuit of claim 1, in which the phase-error-compensation means include means for generating a phase-error-compensation signal from said rounded phase error value, and for using the phase-error-compensation signal for conditioning a phase difference signal indicative of a phase difference between the feedback signal and the reference signal.

6. The fractional-type phase-locked loop circuit of claim 5, in which said means for generating a phase-error-compensation signal has a resolution corresponding to the number of digits of the output binary code.

7. The fractional-type phase-locked loop circuit of claim 6, in which said means for generating a phase-error-compensation signal include digital-to-analog conversion means for generating the phase-error-compensation signal by converting the rounded phase error value defined by the output binary code.

8. The fractional-type phase-locked loop circuit of claim 7, in which the digital-to-analog conversion means include a multibit digital-to analog converter.

9. The fractional-type phase-locked loop circuit of claim 1, in which said frequency divider control means include an accumulator having an accumulator overflow output controlling the frequency division factor of the frequency divider, and in which said input binary code carries a value contained in the accumulator.

10. The fractional-type phase-locked loop circuit of claim 1, in which said frequency divider control means include a sigma-delta modulator for generating a series of frequency divider control values determining a pattern of variation of the frequency division factor of the frequency divider, said series of values being generated starting from an adjustment value fed to the sigma-delta modulator, and in which the phase-error compensation means includes means for generating said input binary code by calculating an incremental value indicative of an incremental phase error according to the conversion factor and the series of frequency divider control values, and calculating the phase error value by accumulating the calculated incremental value.

11. A circuit for compensating for a phase error between first and second signals, comprising:

a truncator operable to receive a first data set having a first length, the first data set corresponding to the phase error, the truncator further operable to modify the first set to produce a second data set, the second set having a second length shorter than the first length; and

a generator coupled to the truncator, the generator operable to generate an error-compensation signal corresponding to the second set.

12. The circuit of claim 11 wherein the truncator comprises a separator operable to separate the first set into first and second portions.

13. The circuit of claim 12 wherein:

the first portion has a third length; and

the truncator further comprises a modifier operable to convert the first portion into a third data set having a fourth length shorter than the third length.

14. The circuit of claim 13 wherein the truncator further comprises a combiner operable to combine the second portion with the third set.

15. The circuit of claim 13 wherein the modifier comprises a delta-sigma modulator.

16. The circuit of claim 11 wherein the generator comprises a digital-to-analog converter.

17. A circuit for compensating for a phase error between first and second signals, comprising:

a separator operable to receive a first data set having a first length, the first data set corresponding to the phase error, the separator further operable to separate the first set into first and second portions, the first portion having a second length;

a modifier coupled to the separator, the modifier operable to convert the first portion into a second data set having a third length shorter than the second length; and

a combiner coupled to the modifier, the combiner operable to combine the second portion with the second set to produce a third data set from which an error-

compensation signal is produced, the third set having a fourth length shorter than the first length.

18. A method of compensating for a phase error between first and second signals, comprising:

receiving a first data set having a first length, the first data set corresponding to the phase error;

producing a second data set from the first set, the second set having a second length shorter than the first length; and

producing an error-compensation signal from the second set.

19. The method of claim 18 wherein producing the second data set comprises separating the first set into first and second portions.

20. The method of claim 19 wherein:

the first portion has a third length; and

producing the second data set further comprises converting the first portion into a third data set having a fourth length shorter than the third length.

21. The method of claim 20 wherein producing the second data set further comprises combining the second portion with the third set.

22. A phase-locked loop, comprising:

a circuit operable to introduce a phase error between first and second signals;

a truncator coupled to the circuit, the truncator operable to receive a first data set having a first length, the first data set corresponding to the phase error, the truncator further operable to modify the first set to produce a second data set, the second set having a second length shorter than the first length; and

a generator coupled to the truncator, the generator operable to generate a compensation signal corresponding to the second set.

23. An electronic system, comprising:

a circuit for compensating for a phase error between first and second signals, comprising:

a truncator operable to receive a first data set having a first length, the first data set corresponding to the phase error, the truncator further operable to modify

the first set to produce a second data set, the second set having a second length shorter than the first length; and

a generator coupled to the truncator, the generator operable to generate a compensation signal corresponding to the second set.